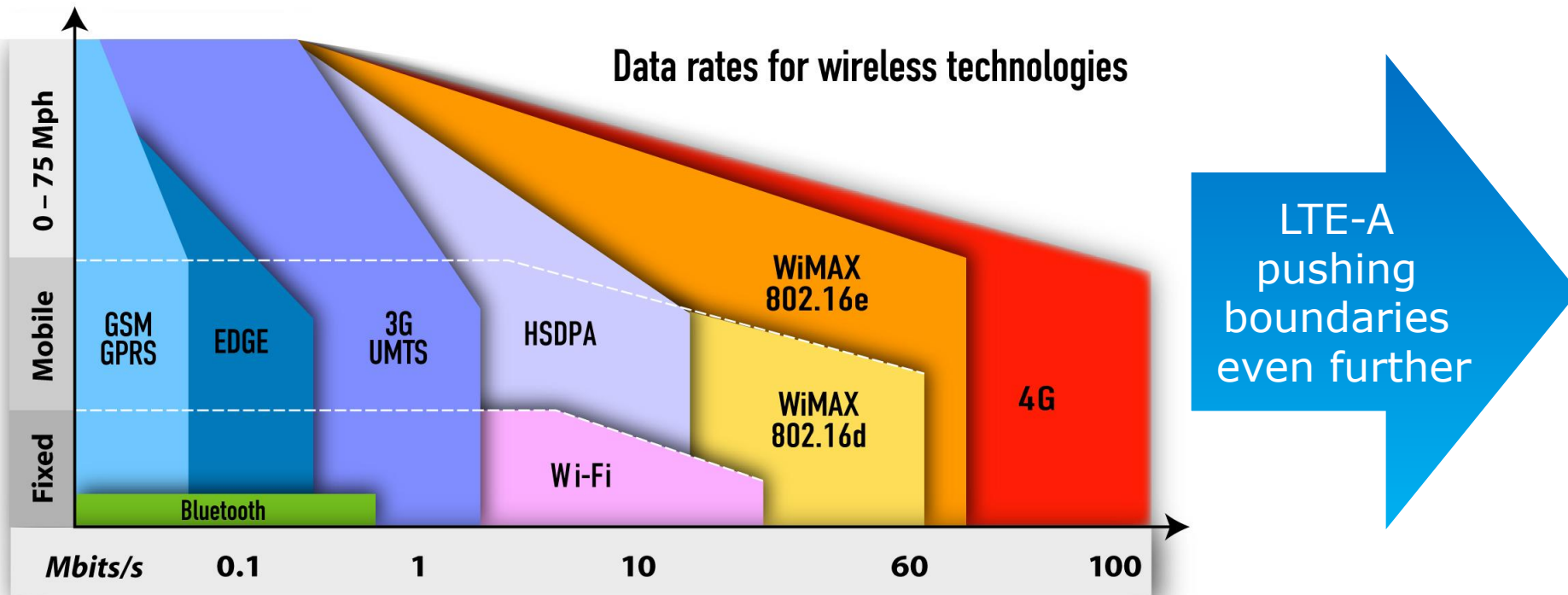




synchronized debugging of heterogeneous processors on an MPSoC for high-speed mobile communications

Uwe Steeb
Nov 2013

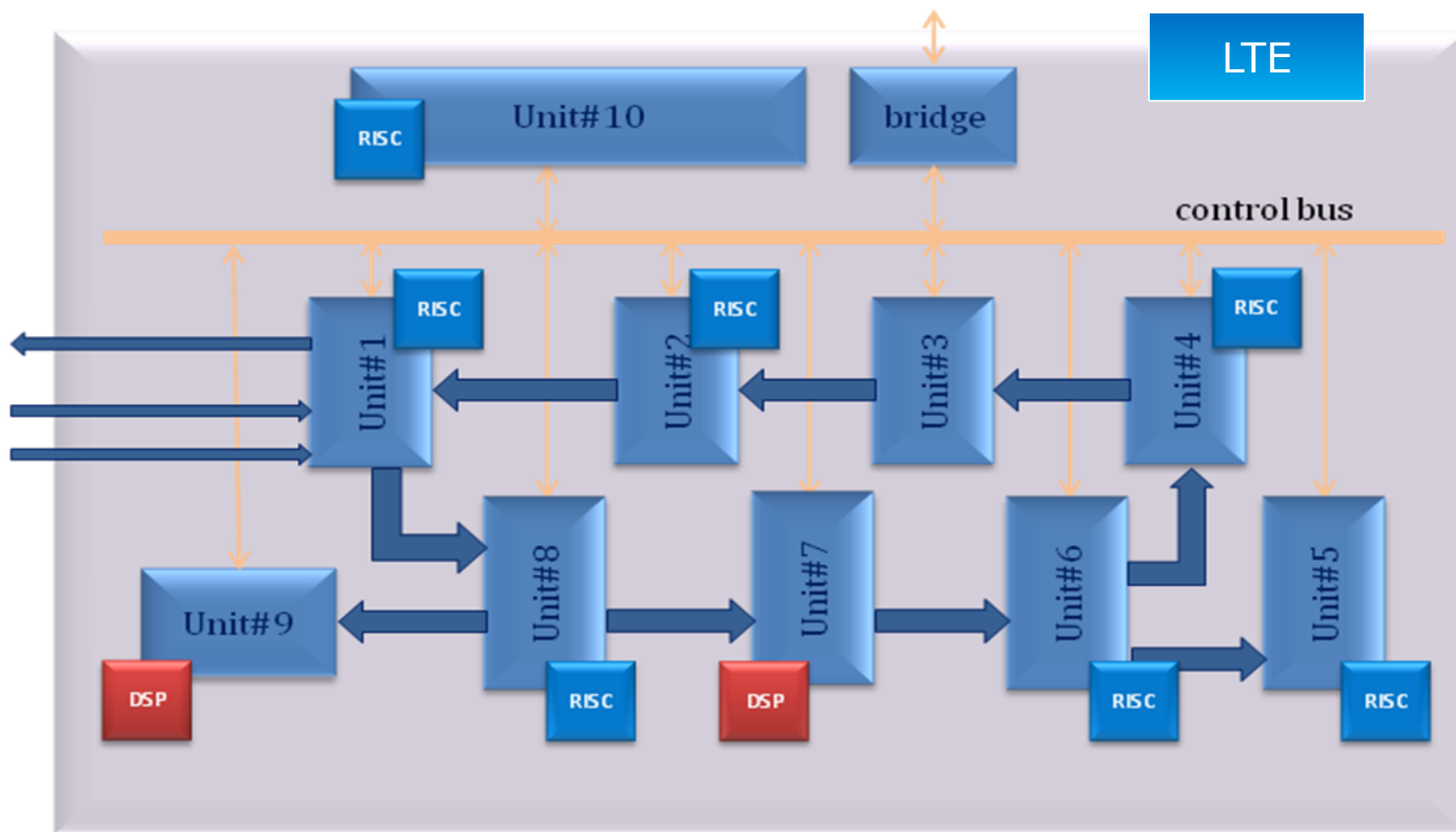
LTE / LTE-A - compute complexity challenge



Sources: WiSOA, Siemens, ABI, Intel, Maravedis, Samsung, UMTS Forum, Nokia

- LTE requires 10 times computational power over HSDPA

Application specific MPSoC Architecture



Debug Approach

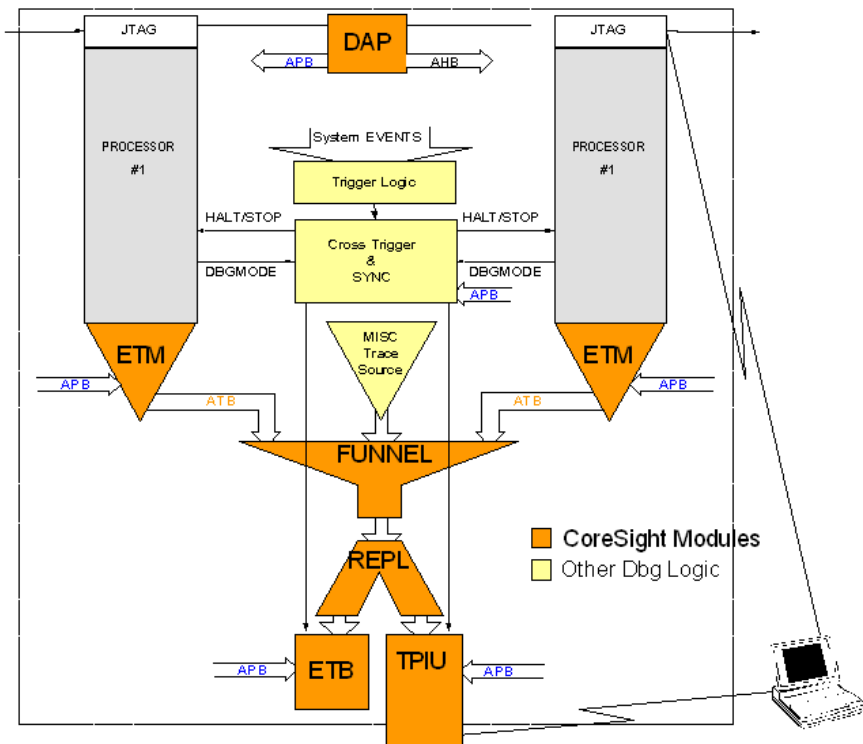
The two main methods to debug an SoC

- Non-Intrusive Debugging / Tracing or Monitoring
 - **PRO:** RealTime / Does not change the behaviour of the System
 - **CON:** limited level of insight / Many Pins / High Bandwidth / High Gate Count
 - **CON:** Expensive Tools / usually available only in small amounts

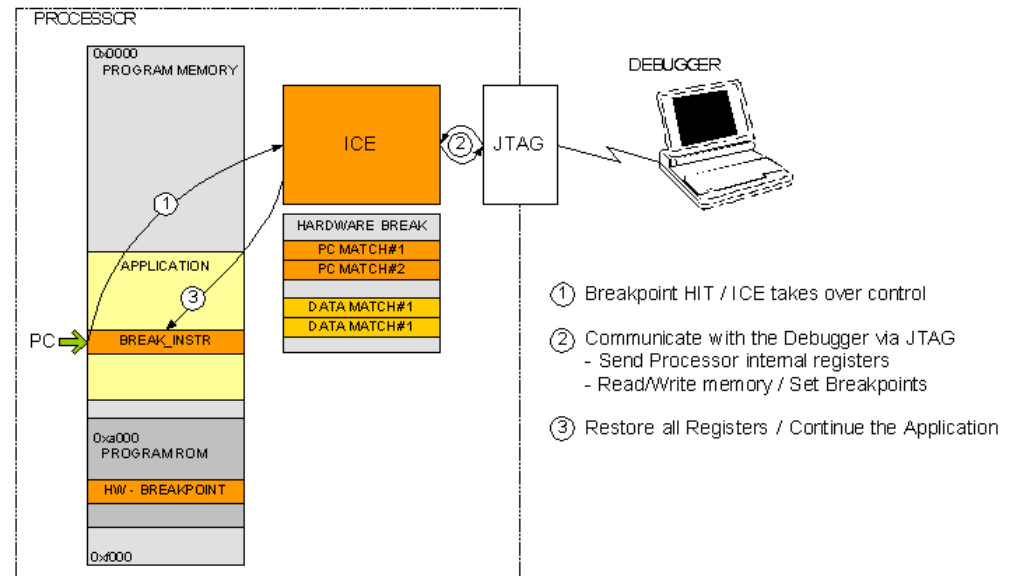
- Intrusive Debugging / Start-Stop-Step debugging
 - **CON:** Not RealTime / Changes the behaviour of the System
 - **PRO:** Deep Insight / small amount of pins / low Gate Count
 - **PRO:** Inexpensive Tools / usually available in large amounts

The two main methods to debug an SoC

Non-Intrusive Tracing



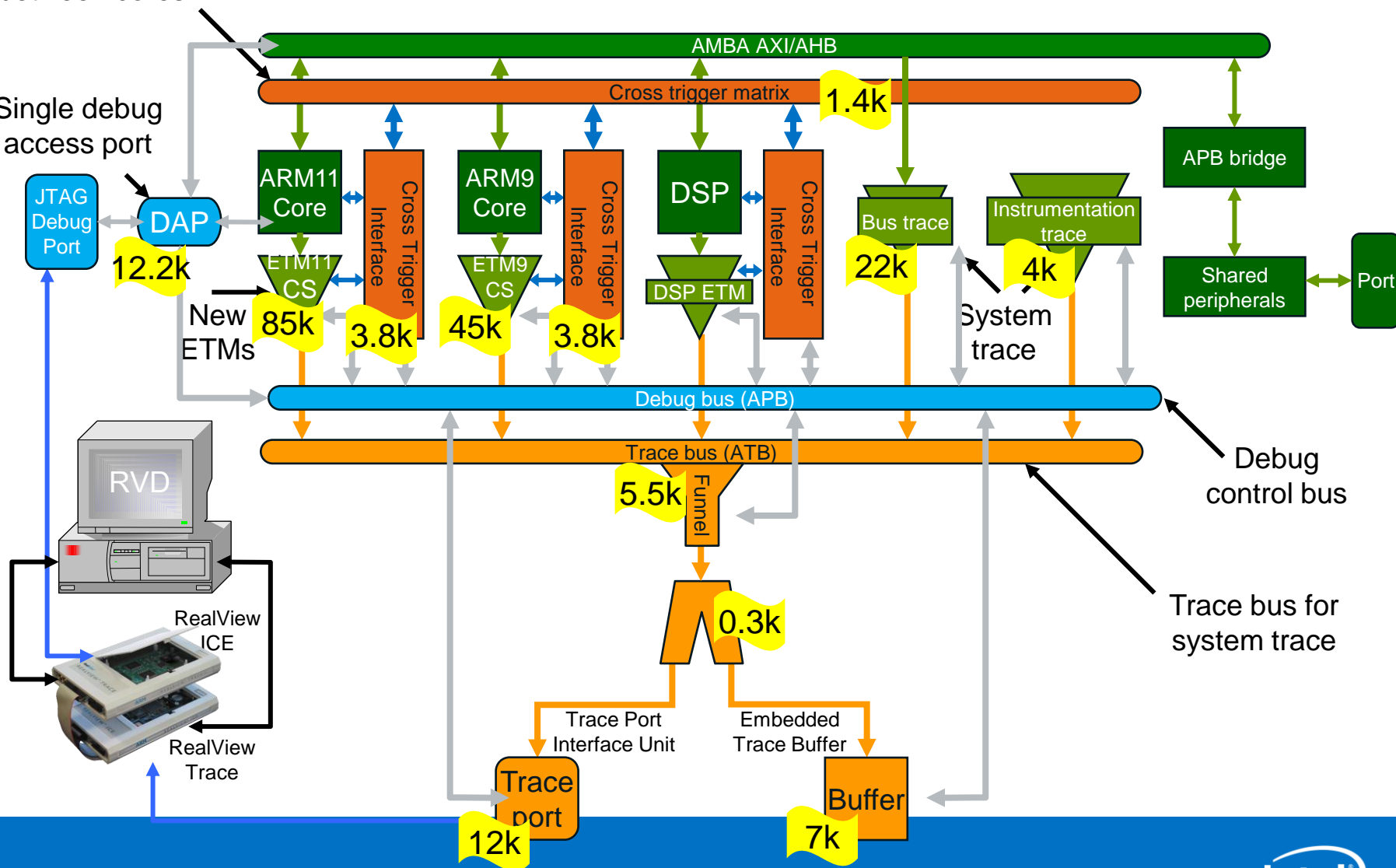
Intrusive Start-Stop debugging



Gate count CoreSight components

Cross triggering between cores

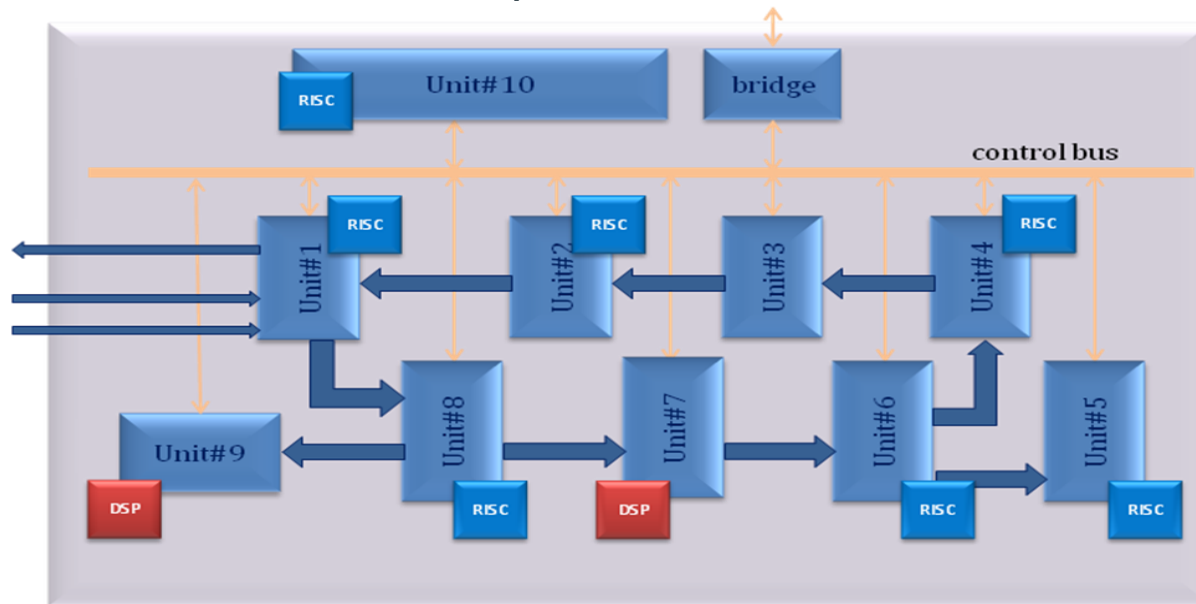
Single debug access port



Intrusive Start/Stop Debugging of an MPSoC

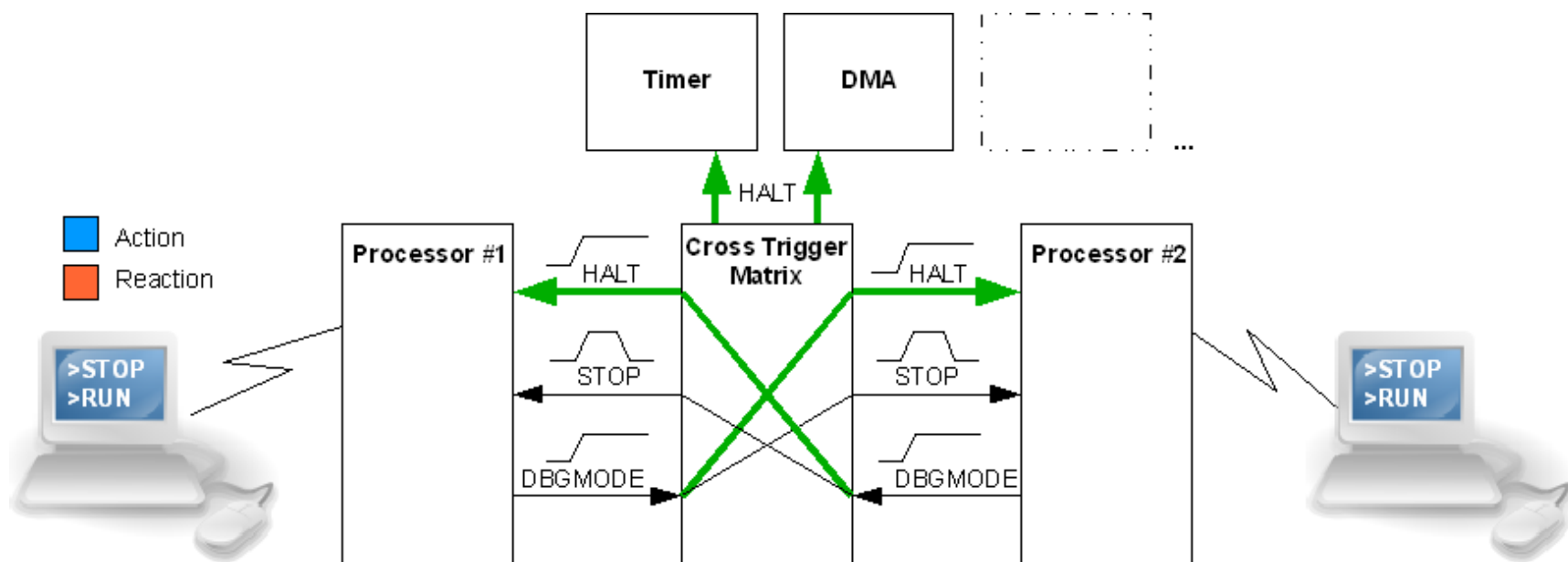
- **PRO:** Very low GateCount / Deep Insight / Inexpensive Tools
- **CON:** Interrupts from other components are missed
- **CON:** Messages from other cores are missed
- **CON:** Buffers with incoming data can overflow

SOLUTION: Freeze all other components while a core is debugged



Cross Connect via Cross Trigger Matrix

How to synchronize processors and peripherals when debugging



DBGMODE signals are asserted while the processor is debugged

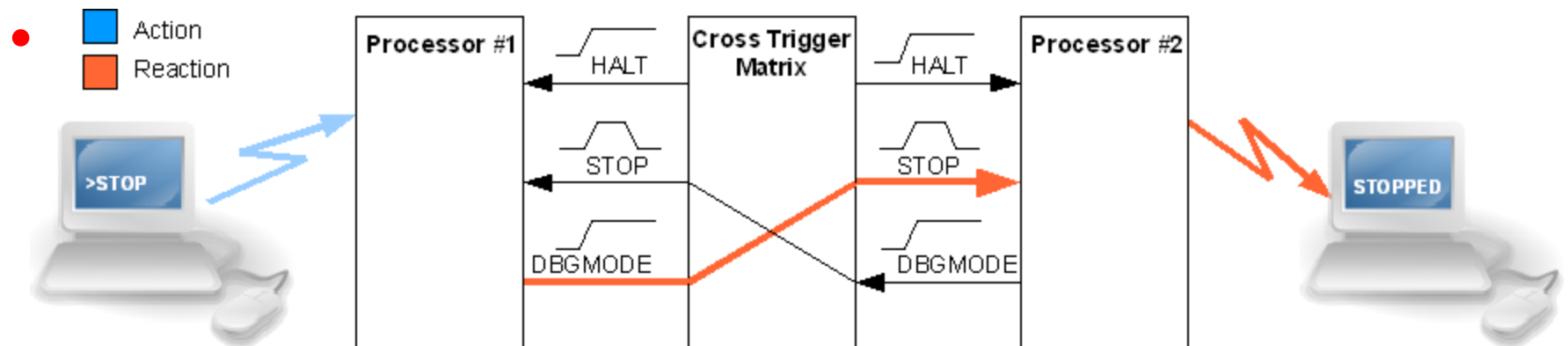
HALT inputs stall the processor when **high**

STOP inputs set the processor in debug mode with a **pulse**

De Facto Industry Standard for Cross Connect has Drawbacks

The Matrix is configured so that **each core STOPS the other**.
I.e. other cores are set in Debug Mode

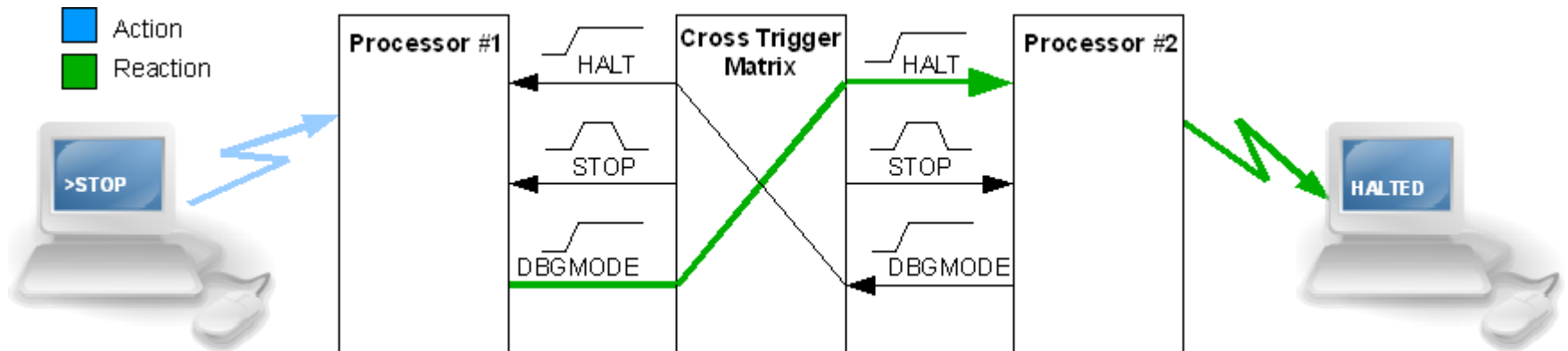
- **CON:** synchronized restart is not standardized and complex
- **CON:** Debug Events and Synchronization Events overlap

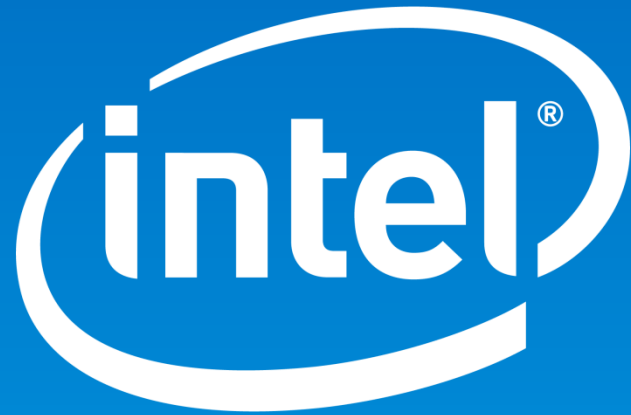


Proposed new Standard

The Matrix is configured so that **each core HALTs the other ...**

- **PRO:** synchronized restart is simple and part of the concept
- **PRO:** Debug Events and Synchronization Events are separated
- **PRO:** Debuggers and Processors from different vendors can be used





Intel Mobile Communications